**IEEE 34 Bus system in Simulink**

* Two models are created, one with lines modelled as Distributed parameters Line (DPL) and other with lines modeled as Pi Section Line(PI)
* Voltage regulators are modelled and includes LDC
* Initial Tap settings are taken same as the benchmark document.
* Runs in Phasor domain. Simulation is much faster compared to the discrete domain simulation.
* ZIP loads are modeled

**Regulator Taps and Parameters**

|  |  |  |  |
| --- | --- | --- | --- |
| Regulator ID: | 1 |  |  |
| Line Segment: | 814 - 850 |  |  |
| Phases: | A - B -C |  |  |
| Connection: | 3-Ph,LG |  |  |
| Monitoring Phase: | A-B-C |  |  |
| Bandwidth: | 2.0 volts |  |  |
| PT Ratio: | 120 |  |  |
| Primary CT Rating: | 100 |  |  |
| Compensator Settings: | Ph-A | Ph-B | Ph-C |
| R - Setting: | 2.7 | 2.7 | 2.7 |
| X - Setting: | 1.6 | 1.6 | 1.6 |
| Voltage Level: | 122 | 122 | 122 |
| Time Delay Assumed(s): | 10 | 10 | 10 |
|  |  |  |  |
| Regulator ID: | 2 |  |  |
| Line Segment: | 852 - 832 |  |  |
| Phases: | A - B -C |  |  |
| Connection: | 3-Ph,LG |  |  |
| Monitoring Phase: | A-B-C |  |  |
| Bandwidth: | 2.0 volts |  |  |
| PT Ratio: | 120 |  |  |
| Primary CT Rating: | 100 |  |  |
| Compensator Settings: | Ph-A | Ph-B | Ph-C |
| R - Setting: | 2.5 | 2.5 | 2.5 |
| X - Setting: | 1.5 | 1.5 | 1.5 |
| Voltage Level: | 124 | 124 | 124 |
| Time Delay Assumed(s): | 15 | 15 | 15 |

**Comparison of Steady state voltages and Substation Power**

|  |  |  |  |
| --- | --- | --- | --- |
| **Substation Active Power (KW)** | **Phase a** | **Phase b** | **Phase c** |
| Benchmark | 759.136 | 666.663 | 617.072 |
| Simulink DPL | 792.7 | 684.8 | 629.3 |
| Simulink PI | 767.7 | 688 | 626.2 |

|  |  |  |  |
| --- | --- | --- | --- |
| **Substation Reactive Power (KVar)** | **Phase a** | **Phase b** | **Phase c** |
| Benchmark | 171.727 | 90.137 | 28.394 |
| Simulink DPL | 175.6 | 95.7 | 27.06 |
| Simulink PI | 193.8 | 111.8 | 53.2 |

|  |  |  |
| --- | --- | --- |
| **Tap Setting** | **Regulator 1** | **Regulator 2** |
| Benchmark | 12 5 5 | 13 11 12 |
| Simulink(Initial) | 12 5 5 | 13 11 12 |
| Simulink(Final) | 15 5 5 | 14 12 12 |

**Phase A Voltage**

****

**Phase B Voltage**

****

**Phase C Voltage**

****

**% Error Voltage**

****

|  |  |  |  |
| --- | --- | --- | --- |
| **Max Error pu** | **Phase a** | **Phase b** | **Phase c** |
| Simulink DPL | 0.0103 | 0.0044 | 0.0066 |
| Simulink PI | 0.0246 | 0.0096 | 0.0 13 |

The main reason for the difference in voltage compared to benchmark is due to the assumptions and approximations taken as given below

* Distributed Load Modeling can cause error as assuming half load at both ends may not be correct.